DATE	REVISION NUMBER	INITIALS	Initial Release
8/11/2013	A0 (EVT V00)	RK	Initial draft
19/03/2014	B0 (DVT V00)	RK	Initial draft. Deleted Programming pin on BT900-A0 and R69, R68, CON18. NOPO R26 (10K). Added R79 100K pull down R80, R82 on BT_PCM_Select. Added 32.768kHz oscillator Y2, R83, R84, C42, R81, CON6. Added 2-pin header CON7, CON8 R67(10K), R68(10K) to push buttons. Added R69 10K pull-up on nRESET line. Changed current shunt monitor IC from 200V/V gain (INA216A4YFFR,TI) to 100V/V gain IC INA216A3YFFR,TI. BT900-B0 module U5 has new pin for input external 32.768kHz oscillator. BT900-B0 module pin order changed. Rewired JP2, JP5, JP3, JP2, CON14 etc..
16/05/2014	1.0 (MP V01)	RK	MP. JP1 (JTAG connector) not fitted (Nopop). J10 wiring correction (to match FTDI cable). Added CON9 (2-pin header) in series with pull-up R75. Changed CON4(USB connector) from MiniUSB-B to MiniUSB-AB. Added jumper (See DIP switch settings sheet in BOM) on CON9 (2-pin header).
29/10/2014 7/11/2014	2.0 (MP V02)		Change R73, R74 from 1K to 150R. Rename BT900 pins: 1). pin35 BT_PCM_OUT,pin36 BT_PCM_SYNC, pin37 BT_PCM_CLK, pin38 BT_PCM_IN to BT_NC. 2). pin22 SIO_19 to SIO_19/(VSP). 3). pin3 nAutoRUN to nAutoRUN/SIO_22. PCB changed from DVK-BT900-V01 to DVK-BT900-V02. V02 PCB corrects for silk screen only: added CON7, CON8 silk screen. correct silk screen for BT900 (U5) to show correct pin numbers.

PCB design specification

1. Substrate: FR4 ROHS compliant, High TG 140 degree.
2. Solder mask, color=BLUE, Silkscreen color=WHITE
3. Surface finish to be Immersion Nickel/Gold (ENIG) with 1-2 u"
4. Start with 1/2 oz. copper on all layers.

ZZ-PCB1

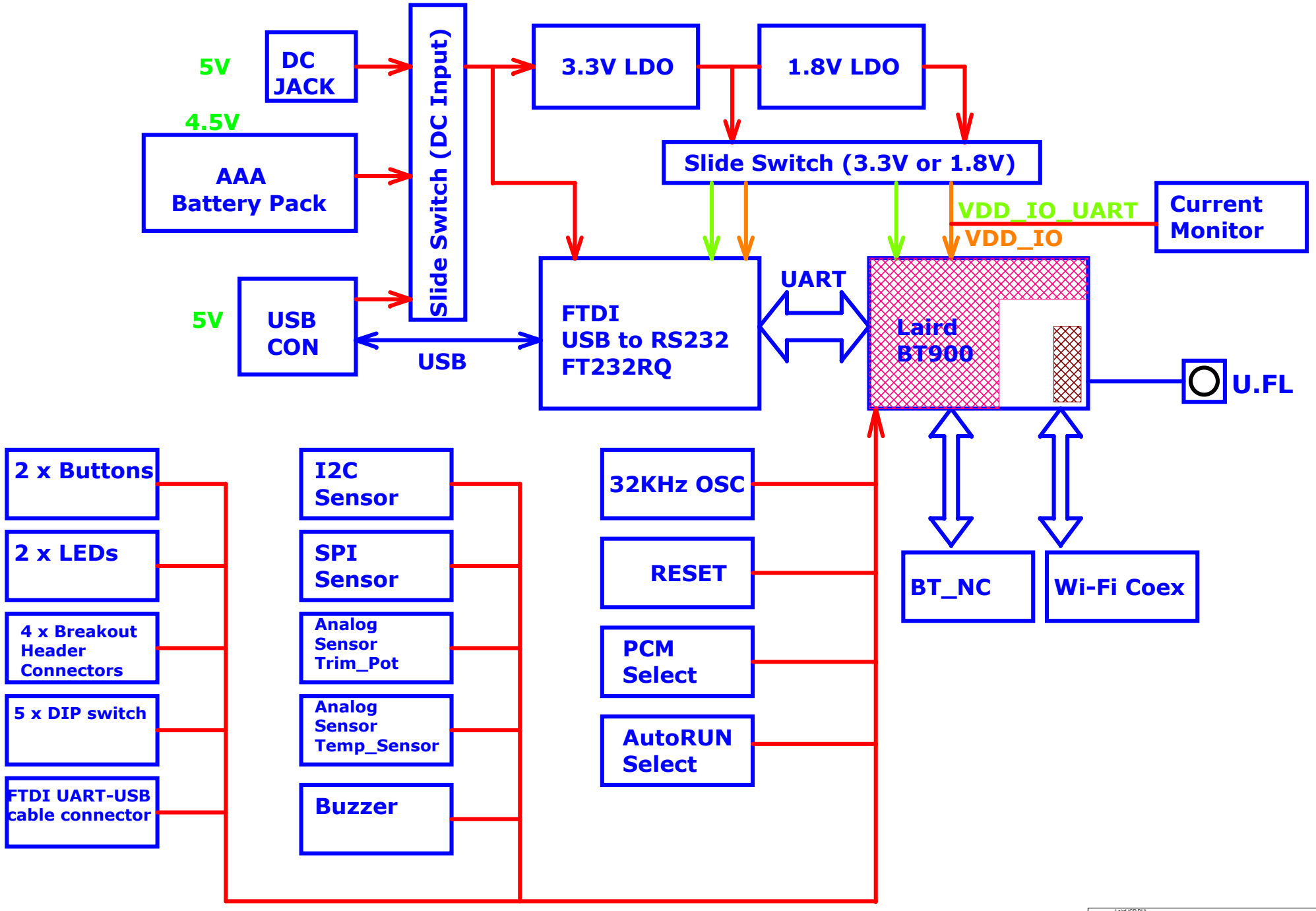
PCB

Laird (CP BU)

Title: BT900 Development Board (DVK-BT900-V02) - History

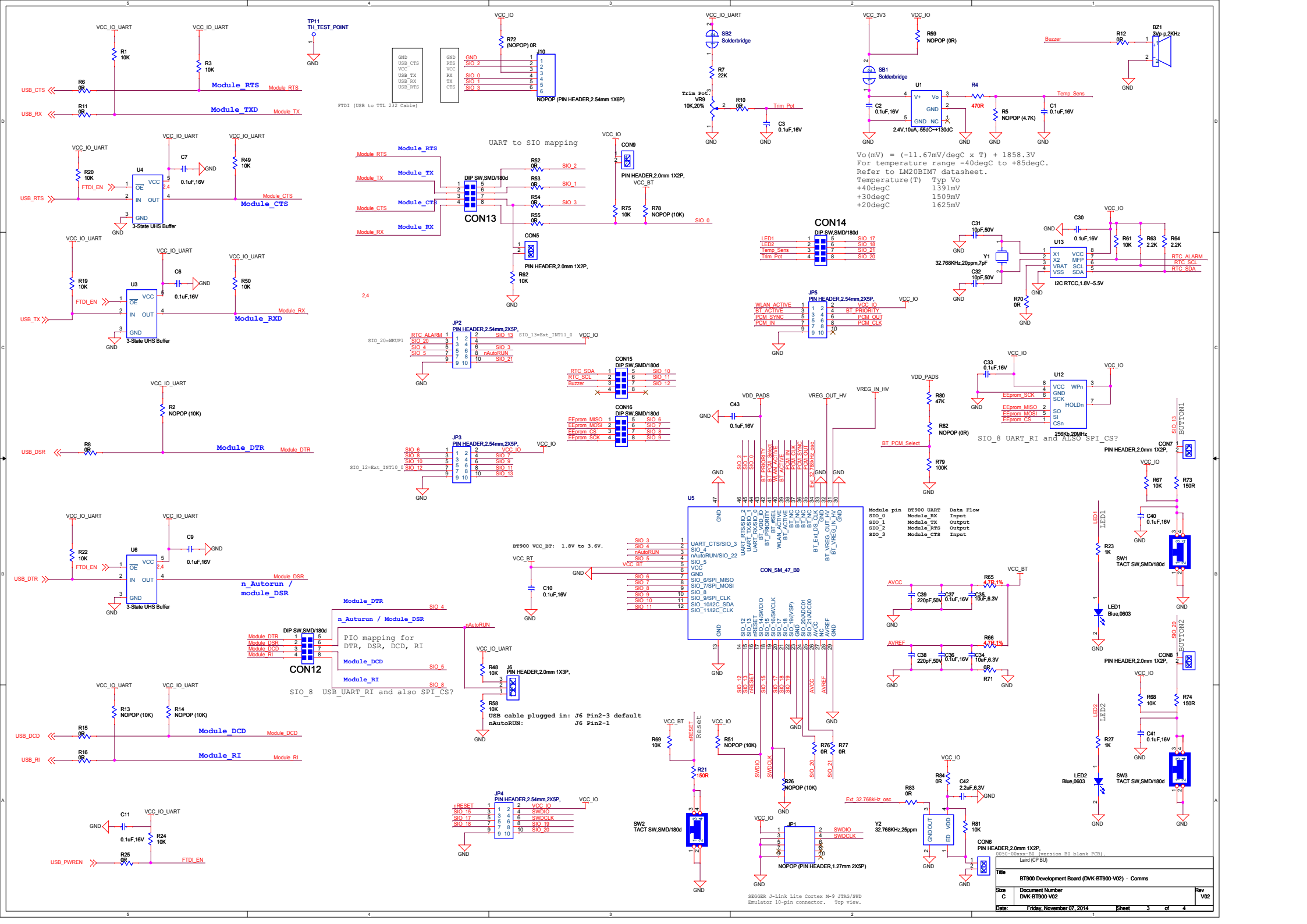
Size: A3 | Document Number: DVK-BT900-V02 | Rev: V02

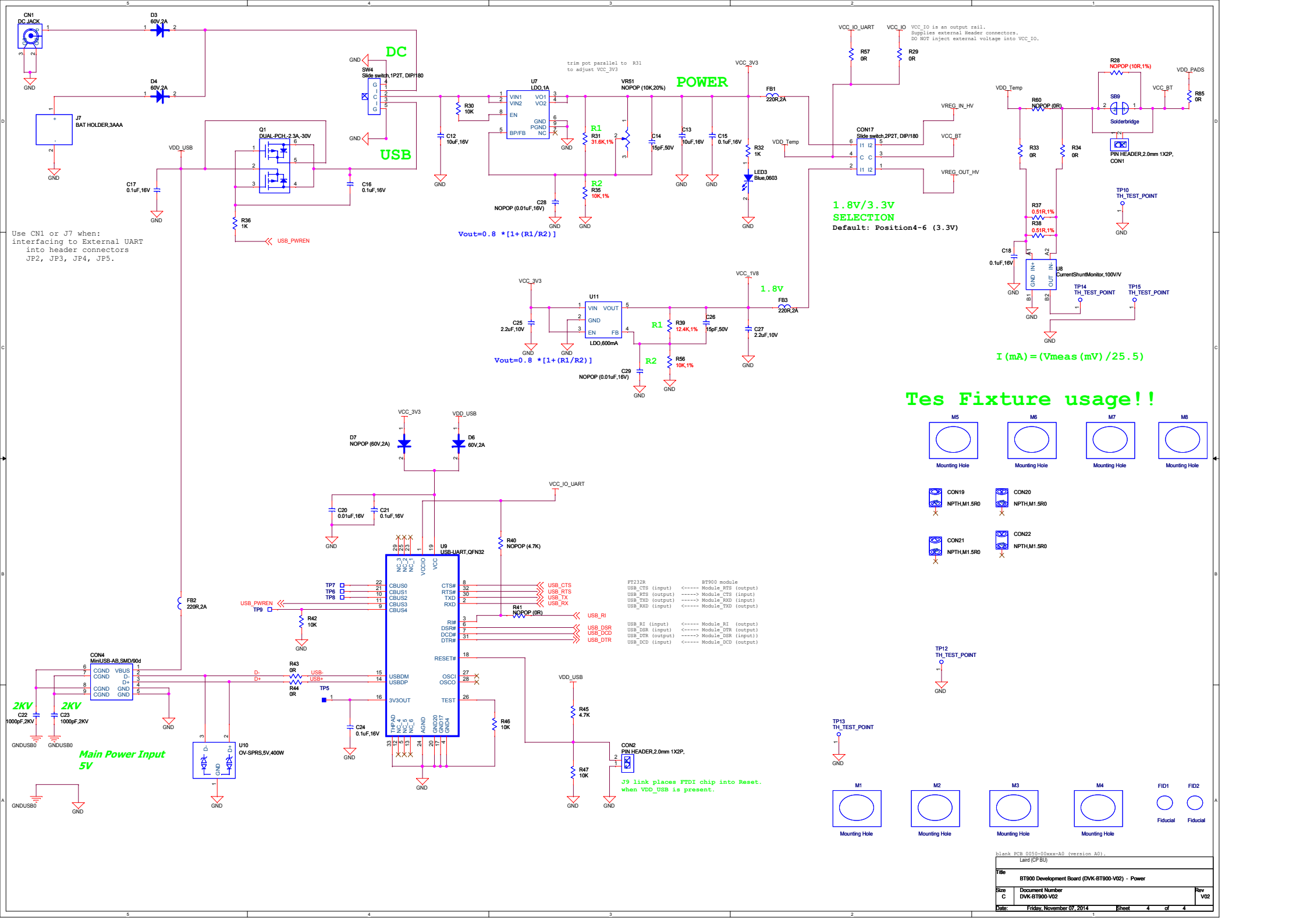
Date: Friday, November 07, 2014 | Sheet 1 of 4



Laird (CP BU)

Title	BT900 Development Board (DVK-BT900-V02) -Block Diagram	
Size C	Document Number DVK-BT900-V02	Rev V02
Date: Friday, November 07, 2014	Sheet 2 of 4	


VCC_IO_UART
R1 10K
R3 10K
Module_RTS
Module_TXD
USB_CTS
USB_RX
R6 0R
R11 0R
TP11
TH_TEST_POINT
FTDI (USB to TTL 232 Cable)
R72 (NOPOP) 0R
J10
NOPOP (PIN HEADER,2.54mm 1X6P)
SB2 Solderbridge
R7 22K
Trim Pot
VR9 10K,20%
R10 0R
C3 0.1uF,16V
SB1 Solderbridge
R59 NOPOP (0R)
U1
2.4V,10uA,-55dC~+130dC
C2 0.1uF,16V
R4 470R
R5 NOPOP (4.7K)
C1 0.1uF,16V
Buzzer
R12 0R
BZ1 3Vp-p,2KHz
Vo(mV) = (-11.67mV/degC x T) + 1858.3V
For temperature range -40degC to +85degC.
Refer to LM20BIM7 datasheet.
Temperature(T) Typ Vo
+40degC 1391mV
+30degC 1509mV
+20degC 1625mV
U4
3-State UHS Buffer
R20 10K
R49 10K
C7 0.1uF,16V
FTDI_EN
USB_RTS
Module_CTS
UART to SIO mapping
DIP SW,SMD/180d
CON13
R52 0R
R53 0R
R54 0R
R55 0R
R75 10K
R78 NOPOP (10K)
CON9
PIN HEADER,2.0mm 1X2P,
CON5
R62 10K
U3
R19 10K
R50 10K
C6 0.1uF,16V
USB_TX
Module_RXD
CON14
DIP SW,SMD/180d
C31 10pF,50V
C32 10pF,50V
Y1 32.768KHz,20ppm,7pF
U13
I2C RTCC,1.8V~5.5V
C30 0.1uF,16V
R61 10K
R63 2.2K
R64 2.2K
R70 0R
RTC_ALARM
RTC_SCL
RTC_SDA
JP5
PIN HEADER,2.54mm,2X5P,
JP2
PIN HEADER,2.54mm,2X5P,
JP3
PIN HEADER,2.54mm,2X5P,
CON15
DIP SW,SMD/180d
CON16
DIP SW,SMD/180d
R2 NOPOP (10K)
R8 0R
USB_DSR
Module_DTR
VDD_PADS
C43 0.1uF,16V
VREG_IN_HV
VREG_OUT_HV
R80 47K
R82 NOPOP (0R)
R79 100K
BT_PCM_Select
U12
256Kb,20MHz
C33 0.1uF,16V
EEprom_SCK
EEprom_MISO
EEprom_MOSI
EEprom_CS
SIO_8 UART_RI and ALSO SPI_CS?
U5
CON_SM_47_B0
Module pin BT900 UART Data Flow
SIO_0 Module_RX Input
SIO_1 Module_TX Output
SIO_2 Module_RTS Output
SIO_3 Module_CTS Input
BT900 VCC_BT: 1.8V to 3.6V.
C10 0.1uF,16V
CON7
PIN HEADER,2.0mm 1X2P,
BUTTON1
SW1 TACT SW,SMD/180d
LED1 Blue,0603
R67 10K
R73 150R
C40 0.1uF,16V
R23 1K
C39 220pF,50V
C37 0.1uF,16V
C35 10uF,6.3V
C38 220pF,50V
C36 0.1uF,16V
C34 10uF,6.3V
R65 4.7R,1%
R66 4.7R,1%
R71 0R
AVCC
AVREF
U6
3-State UHS Buffer
R22 10K
C9 0.1uF,16V
USB_DTR
Module_DSR
n_Autorun / module_DSR
CON12
DIP SW,SMD/180d
Module_DTR
Module_DSR
Module_DCD
Module_RI
PIO mapping for
DTR, DSR, DCD, RI
n_Autorun / Module_DSR
Module_DCD
Module_RI
nAutoRUN
R48 10K
J6
PIN HEADER,2.0mm 1X3P,
R58 10K
USB cable plugged in: J6 Pin2-3 default
nAutoRUN: J6 Pin2-1
CON8
PIN HEADER,2.0mm 1X2P,
BUTTON2
SW3 TACT SW,SMD/180d
LED2 Blue,0603
R68 10K
R74 150R
C41 0.1uF,16V
R27 1K
R13 NOPOP (10K)
R14 NOPOP (10K)
R15 0R
R16 0R
USB_DCD
USB_RI
Module_DCD
Module_RI
C11 0.1uF,16V
R24 10K
R25 0R
USB_PWREN
FTDI_EN
JP4
PIN HEADER,2.54mm,2X5P,
SW2 TACT SW,SMD/180d
R69 10K
R21 150R
R51 NOPOP (10K)
R76 0R
R77 0R
R26 NOPOP (10K)
nRESET
Reset
SWDIO
SWDCLK
JP1
NOPOP (PIN HEADER,1.27mm 2X5P)
SEGGER J-Link Lite Cortex M-9 JTAG/SWD
Emulator 10-pin connector. Top view.
Y2 32.768KHz,25ppm
R83 0R
R84 0R
C42 2.2uF,6.3V
R81 10K
CON6
PIN HEADER,2.0mm 1X2P,
0050-00xxx-B0 (version B0 blank PCB).
Laird (CP BU)
Title
BT900 Development Board (DVK-BT900-V02) - Comms
Size C
Document Number DVK-BT900-V02
Rev V02
Date: Friday, November 07, 2014
Sheet 3 of 4


DC
USB
POWER
Use CN1 or J7 when:
interfacing to External UART
into header connectors
JP2, JP3, JP4, JP5.
Vout=0.8 *[1+(R1/R2)]
1.8V/3.3V
SELECTION
Default: Position4-6 (3.3V)
I(mA)=(Vmeas(mV)/25.5)
Tes Fixture usage!!
Main Power Input
5V
2KV
J9 link places FTDI chip into Reset.
when VDD_USB is present.
Mounting Hole
Fiducial
BT900 Development Board (DVK-BT900-V02) - Power
Laird (CP BU)
DVK-BT900-V02
Friday, November 07, 2014